

AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Currently Amended) For use in association with a backplane of an item of electronic equipment wherein said backplane comprises a common control bus that can access a first number of device card locations, an apparatus capable of allowing said common control bus to access more than said first number of device card locations, said apparatus comprising:

a complex programmable logic device on a circuit board card within said backplane, wherein said complex programmable logic device is coupled to said common control bus, and wherein said complex programmable logic device is capable of coupling each one of a plurality of device locations of one or more devices on said circuit board card to said common control bus in a manner allowing said common control bus to access more than said first number of card locations.

2. (Currently Amended) The system as set forth in Claim 1 wherein said complex programmable logic device controls the access of a device to said common control bus when a device card location of for said device is coupled to said common control bus.

3. (Currently Amended) The system as set forth in Claim 1 wherein said complex programmable logic device couples ~~device locations~~ devices on said circuit board card to said common control bus to allow said common control bus to access a second number of ~~device card~~ locations ~~on said circuit board card~~ through ~~said~~ complex programmable logic devices on each circuit board card within one of the second number of card locations.
4. (Currently Amended) The system as set forth in Claim 3 wherein ~~said second number of~~ ~~device locations on said circuit board card that said common control bus can access through~~ said complex programmable logic device provides access to a number of circuit board cards within said card locations that is greater than said first number of device locations that said common control bus can otherwise access.
5. (Original) The apparatus as set forth in Claim 1 further comprising:
a card processor on said circuit board card within said backplane, said card processor coupled to said common control bus.
6. (Original) The apparatus as set forth in Claim 5 wherein said card processor is coupled to said common control bus through a serial clock line connection and through a serial data line connection.

7. (Currently Amended) The apparatus as set forth in Claim 5 further comprising:
an electrically erasable programmable read only memory on said circuit board card, said electrically erasable programmable read only memory coupled to said common control bus[[:]], wherein said complex programmable logic device controls the access of said electrically erasable programmable read only memory to said common control bus when said electrically erasable programmable read only memory is coupled to said common control bus.
8. (Original) The apparatus as set forth in Claim 7 wherein said electrically erasable programmable read only memory is coupled to said common control bus through a serial clock line connection and through a serial data line connection.
9. (Original) The apparatus as set forth in Claim 7 wherein said complex programmable logic device is coupled to said common control bus through a serial clock line connection and through a serial data line connection.

10. (Currently Amended) The apparatus as set forth in Claim 1 wherein said common control bus comprises a first two wire bus and a second two wire bus, and wherein said apparatus comprises:

a card processor on said circuit board card within said backplane, said card processor coupled to said first two wire bus and to said second two wire bus of said common control bus through metal oxide semiconductor field effect transistor switches; and

an electrically erasable programmable read only memory on said circuit board card, said electrically erasable programmable read only memory coupled to said first two wire bus and to said second two wire bus of said common control bus through metal oxide semiconductor field effect transistor switches; and,

wherein said complex programmable logic device is coupled to said first two wire bus and to said second two wire bus of said common control bus through metal oxide semiconductor field effect transistor switches.

11. (Original) The apparatus as set forth in Claim 10 wherein said complex programmable logic device controls the access of said electrically erasable programmable read only memory to said first two wire bus and to said second two wire bus of said common control bus.

12. (Currently Amended) For use in association with a backplane of an item of electronic equipment wherein said backplane comprises a common control bus that can access a first number of device card locations, a method for allowing said common control bus to access more than said first number of device card locations, said method comprising ~~the steps of:~~

coupling, in a manner allowing said common control bus to access more than said first number of card locations, each one of a plurality of device card locations on said circuit board card to said common control bus through a complex programmable logic device on said a circuit board card at said one of a plurality of card locations; and

controlling the access of a device on said circuit board card to said common control bus with said complex programmable logic device when a device card location of a circuit board containing said device is coupled to said common control bus.

13. (Currently Amended) The method as claimed in Claim 12 further comprising ~~the step of:~~
coupling a second number of device card locations on said circuit board card to said common control bus through a complex programmable logic device on said a circuit board card in each of said second number of card locations.

14. (Currently Amended) The method as set forth in Claim 13 wherein said ~~second number of device locations is one or more devices on a circuit board card within each of said first number of card locations accesses circuit board cards in a number of card locations greater than said first number of device card locations that said common control bus can access not using through said complex programmable logic device.~~

15. (Currently Amended) The method as claimed in Claim 12 further comprising ~~the steps of:~~
coupling a card processor on said circuit board card within said backplane to said common control bus;
providing clock signals to said card processor from a serial clock line coupled to said common data bus;
reading data from said card processor on a serial data line coupled to said common data bus;
and
writing data to said card processor from said serial data line.

16. (Currently Amended) The method as set forth in Claim 12 further comprising the steps of:
coupling a electrically erasable programmable read only memory on said circuit board card
within said backplane to said common control bus;
providing clock signals to said electrically erasable programmable read only memory from
a serial clock line coupled to said common data bus;
reading data from said electrically erasable programmable read only memory on a serial data
line coupled to said common data bus; and
writing data to said electrically erasable programmable read only memory from said serial
data line.

17. (Currently Amended) The method as set forth in Claim 16 further comprising the step of:
controlling the access of said electrically erasable programmable read only memory to said
common control bus with said complex programmable logic device.

18. (Currently Amended) For use in association with a backplane of an item of electronic equipment wherein said backplane comprises a common control bus that can access a first number of device locations, a method for allowing said common control bus to access more than said first number of device locations, said method comprising ~~the steps of~~:

selectively coupling a first device on a circuit board card within said backplane to said common control bus;

coupling a complex programmable logic device on said circuit board card to said common control bus and to said first device, wherein said complex programmable logic device controls selective coupling of said first device on said circuit board card to said common control bus;

receiving data in said complex programmable logic device through a serial data line coupled to said common data bus; and

interpreting instructions in said data to allow said complex programmable logic device to control data access to said first device.

19. (Currently Amended) The method as set forth in Claim 18 further comprising the steps of:
interpreting in said complex programmable logic device a first portion of a first byte of said data to identify a card address for said first device;
interpreting in said complex programmable logic device a second portion of said first byte of said data to identify a device code of said first device; and
interpreting in said complex programmable logic device a third portion of said first byte of said data to identify an instruction to read data or write data to said first device.

20. (Original) The method as set forth in Claim 19 wherein said first device is one of: an electrically erasable programmable read only memory, a card processor, a card status register, and a card control register.